WHAT IS CLAIMED IS:

1. A memory device comprising:

a nonvolatile memory capable of storing data;

a volatile memory capable of being random-accessed; and

a controller for transferring data between said nonvolatile memory and said volatile memory and enabling a pseudo access as if said volatile memory were externally directly accessed in accordance with an instruction through an external bus when the data transfer is not performed.

2. The device according to claim 1, wherein said controller includes a register capable of storing a source address, a destination address, and a size of data to be transferred.

3. The device according to claim 1, wherein said controller performs data transfer between said volatile memory and said nonvolatile memory in accordance with an external instruction without affecting said external bus.

4. The device according to claim 3, wherein said controller notifies said external bus of an end of the data transfer by an interrupt.

5. The device according to claim 1, wherein said controller temporarily stops the data transfer by a suspend command in data transfer between said nonvolatile memory and said volatile memory, accesses said volatile memory in accordance with an external

instruction, and then resume the data transfer by a resume command.

6. The device according to claim 1, wherein said nonvolatile memory, said volatile memory, and said controller are incorporated in a single package.

7. A memory device comprising:

a nonvolatile memory capable of storing data;

a volatile memory capable of being random-accessed; and

a controller capable of starting writing a plurality of data units in said volatile memory or said nonvolatile memory before said plurality of data units have been completely read out from said nonvolatile memory or said volatile memory in data transfer between said nonvolatile memory and said volatile memory.

8. The device according to claim 7, wherein said controller can start writing a plurality of data units in said volatile memory before said plurality of data units have been completely read out from said nonvolatile memory in data transfer from said nonvolatile memory to said volatile memory.

9. The device according to claim 7, wherein said controller can start writing a plurality of data units in said nonvolatile memory before said plurality of data units have been completely read out from said volatile memory in data transfer from said volatile memory to said nonvolatile memory.

10. The device according to claim 7, wherein said controller performs error detection and/or correction processing in said data transfer.

11. The device according to claim 10, wherein said controller reads out actual data and error detection and correction data from said nonvolatile memory, performs error detection and/or correction processing for said actual data on the basis of said error detection and correction data, and writes said actual data in said volatile memory, in data transfer from said nonvolatile memory to said volatile memory.

12. The device according to claim 10, wherein said controller reads out actual data from said volatile memory, generates error detection and correction data on the basis of said actual data, and writes said actual data and said error detection and correction data in said nonvolatile memory, in data transfer from said volatile memory to said nonvolatile memory.

13. The device according to claim 10, wherein said controller includes an error detection and correction register for storing error detection and correction information.

14. The device according to claim 13, wherein said error detection and correction register stores an address of data from which an error has been detected.

15. The device according to claim 7, wherein

said controller includes a buffer for buffering data and performs said data transfer through said buffer.

16. The device according to claim 15, wherein said controller performs said data transfer in a time obtained by adding one transfer cycle to a time obtained by multiplying a transfer cycle by the number of transfer data.

17. The device according to claim 16, wherein said controller reads out actual data and error detection and correction data from said nonvolatile memory, performs error detection for said actual data on the basis of said error detection and correction data, writes said actual data in said volatile memory, and performs error correction processing for said actual data on said volatile memory, in data transfer from said nonvolatile memory to said volatile memory.

18. A memory device comprising:

a plurality of memories having different electrical specifications; and

a controller including a memory bus connected to said plurality of memories and an external bus externally connected, said external bus having a single input/output voltage level, said memory bus and said external bus having different input/output voltage level ranges.

19. The device according to claim 18, wherein said plurality of memories have different operable input/output voltage level ranges.

20. The device according to claim 19, wherein said controller accesses said plurality of memories using an overlap range of the operable input/output voltage levels of said plurality of memories.

21. The device according to claim 20, wherein said controller comprises a power supply terminal for inputting a power supply voltage at an input/output voltage level within said overlap range and controls an input/output voltage levels of said plurality of memories on the basis of a voltage of said power supply terminal.

22. The device according to claim 19, wherein said controller accesses said plurality of memories using different input/output voltage levels which do not overlap.

23. The device according to claim 22, wherein said controller comprises two power supply terminals for inputting power supply voltages at different input/output voltage levels which do not overlap and controls input/output voltage levels of said plurality of memories on the basis of voltages of said two power supply terminals.

24. The device according to claim 22, wherein operable input/output voltage level ranges of said plurality of memories do not overlap.

25. The device according to claim 18, wherein said plurality of memories includes a nonvolatile memory and a volatile memory.

26. A memory device comprising:

a nonvolatile memory including an actual data area for storing a plurality of actual data units and a spare data area for storing a plurality of spare data units;

a volatile memory including an actual data area for storing a plurality of actual data units and a spare data area for storing a plurality of spare data units; and

a controller for performing data transfer between said nonvolatile memory and said volatile memory.

27. The device according to claim 26, wherein each of said spare data units includes control information or management information.

28. The device according to claim 26, wherein said plurality of actual data units and said plurality of spare data units are in a one-to-one correspondence.

29. The device according to claim 26, wherein said actual data area and said spare data area in said volatile memory are provided as continuous address areas.

30. The device according to claim 29, wherein said actual data area and said spare data area in said nonvolatile memory are provided as discontinuous address areas.

31. The device according to claim 28, wherein said controller decomposes actual and spare data

units which have been correspondingly read out from said actual data area and said spare data area in said nonvolatile memory, and writes the discomposed actual and spare data units respectively in said actual data area and said spare data area in said volatile memory, in data transfer from said nonvolatile memory to said volatile memory.

32. The device according to claim 28, wherein said controller includes a first write controller for linking actual and spare data units which have been correspondingly read out from said actual data area and said spare data area in said volatile memory, and writing the linked actual and spare data units respectively in said actual data area and said spare data area in said nonvolatile memory, in data transfer from said volatile memory to said nonvolatile memory.

33. The device according to claim 28, wherein said controller includes a spare data register for storing one or more spare data units, links an actual data unit in said actual data area in said volatile memory and a spare data unit in said spare data register, and writes the linked actual and spare data units respectively in said actual data area and said spare data area in said nonvolatile memory.

34. The device according to claim 33, wherein said spare data register is for storing one spare data unit.

35. The device according to claim 33, wherein said controller writes a plurality of spare data units in said nonvolatile memory using one spare data unit in said spare data register when said plurality of spare data units have the same contents.

36. The device according to claim 32, wherein said controller includes a second write controller including a spare data register for storing one or more spare data units, said second write controller linking an actual data unit in said actual data area in said volatile memory and a spare data unit in said spare data register and writing the linked actual and spare data units respectively in said actual data area and said spare data area in said nonvolatile memory.

37. The device according to claim 36, wherein said controller can select which of said first and second write controllers is used to write.

38. The device according to claim 1, wherein

said nonvolatile memory includes a plurality of terminals,

said controller includes a plurality of internal terminals connected to the plurality of terminals of said nonvolatile memory, a plurality of external terminals which can be connected to the outside, and an assign terminal for externally receiving an assign signal, and

when said assign signal is input to said assign

terminal, said controller assigns the plurality of internal terminals for the plurality of external terminals.